WPMDB1400362Q / 171040302

Magl³C Power Module

VDRM – Variable Step Down Regulator Module

2.95 – 6V / 4A / 0.8 – 3.6V Output

DESCRIPTION

The Magi3C 171020302, 171040302 and 171060302 Power Module family provide a fully integrated DC-DC power supply including the switching regulator, regulation loop, power mosfets and shielded inductor in one package. This modules require as few as 3 external components

The 171040302 offers high efficiency and delivers up to 4A of output current. It operates from 2.95 to 6V input voltage and is designed for fast transient response.

It is available in a standard industrial high power density QFN package (11mm x 9mm x 2.8mm) with very good thermal performance.

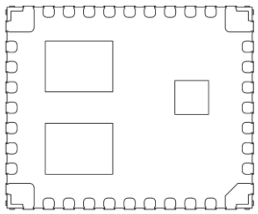
This module has an on-board protection circuitry to guard against thermal overstress and electrical damage featuring thermal shut-down, over-current, short-circuit, over-voltage and under-voltage protections.

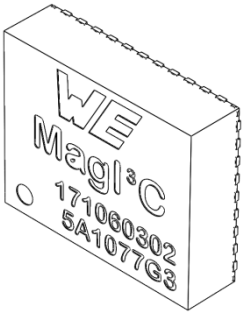
FEATURES

- Peak efficiency up to 96%
- Current capability up to 4A
- Output voltage range: 0.8 to 3.6V
- Current Mode control
- Synchronuos operation
- 1% reference accuracy over temperature
- Adjustable switching frequency (0.5 to 2 MHz)
- Continuous output power: 14.4W
- No derating within the operating temperature range
- Integrated shielded inductor
- Under-voltage lockout protection
- Programmable soft-start and voltage tracking
- Frequency synchronization to external clock
- Thermal shutdown
- Operating ambient temperature up to 85°C
- Inrush current protection
- Adjustable soft start and sequencing
- Cycle by cycle short circuit protection
- Under-voltage and over-voltage Power Good
- Pin compatible with WE171040302 & WE171060302
- Complies with EN55022 class B radiated emissions standard

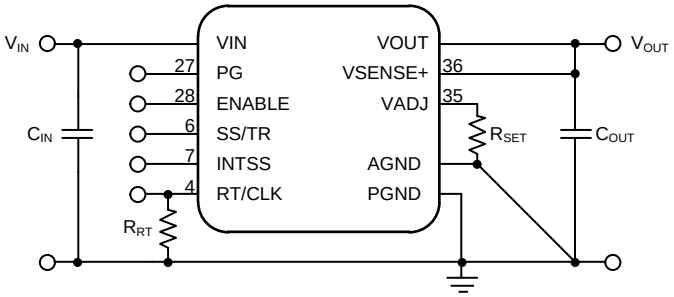
TYPICAL APPLICATIONS

- Point-of-load DC-DC applications from 5V and 3.3V rails
- Industrial, test & measurement, medical applications
- System power supplies
- DSPs, FPGAs, MCUs and MPU supply
- I/O interface power supply
- Communication infrastructure
- High density distributed power systems





TYPICAL CIRCUIT DIAGRAM



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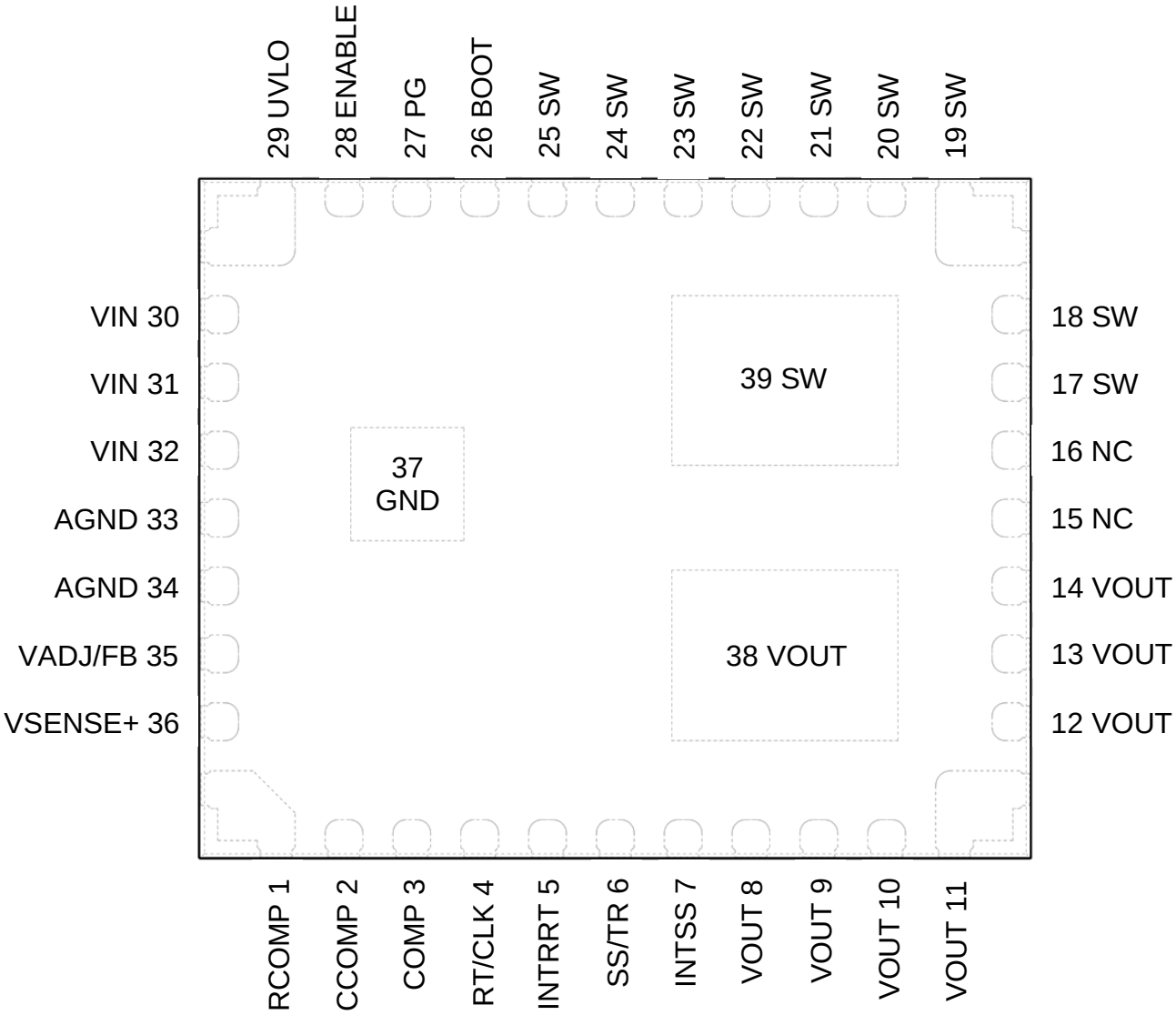
PACKAGE



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PIN DESCRIPTION

SYMBOL	PIN	TYPE	DESCRIPTION
V_{IN}	30,31,32	Power	Input Voltage. Place input capacitors as close as possible
V_{OUT}	8,9,10,11, 12,13,14,38	Power	Output voltage. Place output capacitors as close as possible. For thermal performance use copper plane(s) at these pins.
AGND	5,7,33,34	Supply	Analog ground for internal circuitry. Connect to power ground
PGND	37	Power	Power ground for the internal switching circuitry. Connect to copper plane(s) with thermal vias for thermal performance.
V_{SENSE+}	36	Input	Connect to positive terminal of the output capacitor. An internal resistor of 1430 Ω is connected internally between V_{SENSE+} and V_{ADJ}. This is the upper resistor of the feedback voltage divider.
V_{ADJ}	35	Input	A resistor (R_{SET}) from V_{ADJ} to AGND is needed to select the output voltage. This is the lower resistor of the feedback voltage divider.
RT/CLK	4	Input	An external resistor from RT/CLK to AGND adjusts the switching frequency of the device.
$INTR_{RT}$	5	analog	Internal resistor which defines the default switching frequency.
R_{COMP}	1	analog	Internal resistor of the compensation network. Must be connected to AGND.

OPTIONAL

SYMBOL	PIN	TYPE	DESCRIPTION
UVLO	29	Input	An internal under-voltage lock out resistor of 34kΩ is connected to the enable pin. If connected to analog ground, the internal UVLO resistor divider will be activated. For input voltages below 3.3V this pin should be left open and optional a resistor from enable to analog ground sets the UVLO to values between 2.95 and 3.3 V.
ENABLE	28	Input	Enable pin. Internally pull up source. Pull to analog ground to disable. Float to Enable.
PGOOD	27	Output	Open drain output. The PGOOD pin pulls low during thermal shutdown, over-current, output over-voltage or under-voltage or disabled device. A pull up resistor is required.
SS/TR	6	Input	Internal current source. Connect an external capacitor to optionally increase the soft start time. A voltage applied to this pin allows tracking and sequencing.
INTSS	7	analog	An internal 3.3nF capacitor is connected to this pin. If pin 7 is connected to analog ground, a 1.1ms soft start time is selected.

AUXILIARY

SYMBOL	PIN	TYPE	DESCRIPTION
COMP	3	Output	Output of the error amplifier. If an external compensation is used, pin 1 must be left open.
C_{COMP}	2	analog	Internal capacitor of the compensation network. Do not connect.
BOOT	26	Supply	Internal bootstrap pin for the high side mosfet.
SWITCH	17,18,19,20 ,21,22,23, 24,25,39	Power	Internal switch node. Do not connect these pins.
NC	15,16		Not connected to internal circuitry.

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ORDERING INFORMATION

ORDER CODE	PART DESCRIPTION	SPECIFICATIONS	PACKAGE	PACKAGING UNIT
171040302	WPMDB1400362Q	4A / 14.5W version	BQFN-39	Tape and Reel with 250 units

PIN COMPATIBLE FAMILY MEMBERS

ORDER CODE	PART DESCRIPTION	SPECIFICATIONS	PACKAGE	PACKAGING UNIT
171020302	WPMDB1200362Q	2A / 7.2W version	BQFN-39	Tape and Reel with 250 units
171060302	WPMDB1600362Q	6A / 21.6W version	BQFN-39	Tape and Reel with 250 units

PACKAGE SPECIFICATIONS

Weight	Flammability	MTBF
0.85g	Meets UL 94 V-O	32.8Mhrs, Bellcore TR-332, 50% stress, T_A=40°C, ground benign

SALES INFORMATION

SALES CONTACTS
Würth Elektronik eiSos GmbH & Co. KG EMC & Inductive Solutions Max-Eyth-Str. 1 74638 Waldenburg Germany Tel. +49 (0) 7942 945 0 www.we-online.com powermodules@we-online.com

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ABSOLUTE MAXIMUM RATINGS

Caution:
Exceeding the listed absolute maximum ratings may affect the device negatively and may cause permanent damage.

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN (1)	MAX (1)	
V_{IN}	Input voltage	-0.3	7	V
V_{OUT}	Output voltage	-0.6	V_{IN}	V
V_{ADJ}	Feedback voltage	-0.3	3	V
UVLO	Under-voltage lockout pin voltage	-0.3	3.3	V
EN	Enable pin Voltage	-0.3	7	V
	Enable source current	-	100	µA
RT/CLK	RT/CLK pin voltage	-0.3	6	V
	RT/CLK source current	-	±100	µA
SS/TR	SS/TR pin voltage	-0.3	3	V
	SS/TR pin sink current	-	±100	µA
PGOOD	Power Good pin voltage	-0.3	7	V
	Power Good sink current	-	10	mA
COMP	Output of the error amplifier	-0.3	3	V
	COMP sink current	-	100	µA
INTSS	Internal soft start capacitor	-0.3	3	V
INTRRT	Internal resistor for the initial switching frequency	-0.3	6	V
R_{COMP}	Resistor of the compensation network	-0.3	3	V
C_{COMP}	Capacitor of the compensation network	-0.3	3	V
V_{SENSE+}	Sense for the output voltage.	-0.3	V_{out}	V
V_{SW}	Switch node voltage	-0.6	7	V
SW	10ns transient	-2	7	V
BOOT	Internal supply for the high mosfet driver	-	V_{SW} +8V	V
$T_{storage}$	Storage temperature	-65	150	°C
T_{SOLR}	Peak case/leads temperature during reflow soldering, max. 30sec. (JEDEC J-STD020) Maximum three cycles!	-	245±5	°C
Mechanical shock: Mil-STD-883D, Method 2002.2, 1ms, ½ sine, mounted		-	1500	G
Mechanical vibration: Mil-STD-883D, Method 2007.2, 20-2000Hz		-	20	G

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OPERATING CONDITIONS

Operating conditions are conditions under which operation of the device is intended to be functional. All values are referenced to GND.

MIN and MAX limits are valid for the recommended ambient temperature range of **-40°C to 85°C**. Typical values represents statistically the utmost probability at following conditions: V_{IN} = 3.3V, V_{OUT} = 1.8V, I_{OUT} = 2A, C_{IN1} = 47µF ceramic, C_{IN2} = 220µF poly-tantalum, C_{OUT1} = 47µ ceramic, C_{OUT2} = 100µF poly-tantalum unless otherwise noted.

SYMBOL	PARAMETER	MIN (1)	TYP (2)	MAX (1)	UNIT
V_{IN}	Input voltage	2.95	-	6	V
V_{OUT}	Output voltage (depending on input voltage and switching frequency)	0.8	-	3.6	V
T_A	Ambient temperature range	-40	-	85 (3)	°C
T_{JOP}	Junction temperature range	-40	-	125	°C

THERMAL SPECIFICATIONS

SYMBOL	PARAMETER	TYP (2)	UNIT
Θ_{JA}	Junction-to-ambient thermal resistance (4)	12	°C/W
Ψ_{JT}	Junction-to-top(5)	2.2	°C/W
Ψ_{JB}	Junction-to-board(6)	9.7	°C/W
T_{SD}	Thermal shutdown, rising	175	°C
	Thermal shutdown hysteresis, falling	15	°C

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ELECTRICAL SPECIFICATIONS

MIN and MAX limits are valid for the recommended ambient temperature range of **-40°C to 85°C**. Typical values represents statistically the utmost probability at following conditions: V_{IN} = 3.3V, V_{OUT} = 1.8V, I_{OUT} = 2A, C_{IN1} = 47µF ceramic, C_{IN2} = 220µF poly-tantalum, C_{OUT1} = 47µ ceramic, C_{OUT2} = 100µF poly-tantalum unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNIT
Output current						
I_{OCP}	Output current protection		-	7	-	A
Accuracy						
V_{REF}	Internal accuracy	T_A = 25°C, I_{OUT} = 0A with internal feedback resistor	-	-	±1(7)	%
	Temperature variation	-40°C≤T_A≤85°C, I_{OUT} = 0A	-	±0.3	-	%
V_{OUT}	Line regulation	Over V_{IN} range, T_A = 25°C, I_{OUT} = 0A	-	±0.1	-	%
	Load regulation	Over I_{OUT} range, T_A = 25°C	-	±0.1	-	%
	Total output voltage variation		-	-	±1.5	%
	Output voltage ripple	10µF ceramic, 20MHz BW (8)	-	9	-	mV_{pp}
Switching frequency						
f_{SW}	Switching frequency	Using RT mode	500	-	2000	kHz
		RT/CLK pin open	400	500	600	kHz
f_{CLK}	Synchronization clock frequency range	Using CLK mode	500	-	2000	kHz
	Minimum CLK pulse width		75	-	-	ns
V_{CLK-H}	RT/CLK high threshold	Relative to AGND	2.2	-	3.3	V
V_{CLK-L}	RT/CLK low threshold		-0.3	-	0.4	V
f_{CLK}	RT/CLK to switch node delay		-	90	-	ns
	PLL lock-in-time		-	14	-	µs
Enable and under-voltage lockout						
V_{UVLO}	V_{IN} under-voltage threshold	V_{IN} increasing, UVLO pin connected to AGND	-	3.05	3.135	V
		V_{IN} decreasing, UVLO pin connected to AGND	2.5	2.75	-	V
V_{ENABLE}	Enable threshold trip point	Enable logic high voltage	-	1.25	-	V
		Enable logic low voltage	-0.3	-	1.0	V
Power Good						
PG	Power Good threshold	V_{OUT} rising, V_{OUT} GOOD	-	93	-	%
		V_{OUT} rising, V_{OUT} FAULT	-	107	-	%
		V_{OUT} falling, V_{OUT} GOOD	-	105	-	%
		V_{OUT} falling, V_{OUT} FAULT	-	91	-	%
	Power Good low voltage	I_{PG} = 0.33mA	-	-	0.3	V

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SYMBOL	PARAMETER		TEST CONDITIONS	MIN [1]	TYP [2]	MAX [1]	UNIT
Efficiency							
η	Efficiency	V_{IN} = 5V I_{OUT} = 1A	V_{OUT} = 3.3V, f_{SW} = 1.0MHz	-	95	-	%
			V_{OUT} = 2.5V, f_{SW} = 1.0MHz	-	93	-	%
			V_{OUT} = 1.8V, f_{SW} = 1.0MHz	-	91	-	%
			V_{OUT} = 1.5V, f_{SW} = 1.0MHz	-	89	-	%
			V_{OUT} = 1.2V, f_{SW} = 750kHz	-	97	-	%
			V_{OUT} = 1.0V, f_{SW} = 650kHz	-	85	-	%
			V_{OUT} = 0.8V, f_{SW} = 650kHz	-	84	-	%
		V_{IN} = 3.3V I_{OUT} = 1A	V_{OUT} = 1.8V, f_{SW} = 1.0MHz	-	90	-	%
			V_{OUT} = 1.5V, f_{SW} = 1.0MHz	-	88	-	%
			V_{OUT} = 1.2V, f_{SW} = 750kHz	-	87	-	%
			V_{OUT} = 1.0V, f_{SW} = 650kHz	-	84	-	%
			V_{OUT} = 0.8V, f_{SW} = 650kHz	-	82	-	%
Input and output capacitors							
C_{IN}	External input capacitor		ceramic	47 [9]	-	-	µF
			Non ceramic	-	220 [9]	-	µF
C_{OUT}	External output cpacitor		ceramic	47 [10]	150	650 [11]	µF
			Non ceramic	-	100 [10]	2000 [11]	µF
	Output capacitor ESR			-	-	25	mΩ
Transient Response							
T_{TR}	Transient Response		Recovery time 1A/µs load step from 1.0A to 3A	-	80	-	µs
T_{TR}			V_{OUT} over/undershoot 1A/µs load step from 1.0A to 3A	-	90	-	mV
Input standby current							
I_Q	Input quiescent current		Enable logic low	-	70	100	µA

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NOTES

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.

(2) Typical numbers are valid at 25°C ambient temperature and represent statistically the utmost probability assuming the Gaussian distribution.

(3) Depending on heat sink design, number of PCB layers, copper thickness and air flow.

(4) Measured on a 100 x 100mm two layer board, with 35µm (1 ounce) copper, no air flow

(5) The junction-to-top characterization parameter, Ψ_{JT}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \Psi_{JT} * P_{dis} + T_T$; where P_{dis} is the power dissipated in the device and T_T is the temperature of the top of the device.

(6) The junction-to-board characterization parameter, Ψ_{JB}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \Psi_{JB} * P_{dis} + T_B$; where P_{dis} is the power dissipated in the device and T_B is the temperature of the board 1mm from the device.

(7) The stated limit of the set-point voltage tolerance includes the tolerance of both the internal voltage reference and the internal adjustment resistor. The overall output voltage tolerance is affected by the tolerance of the external RSET resistor.

(8) The industry standard for comparison of the output voltage ripple between switching regulators or modules requires a 10µF ceramic (sometimes additional 1µF ceramic in parallel) at the point of load where the voltage measurement is done using an oscilloscope with its probe and probe jack for low voltage/high frequency (low impedance) measurement. The oscilloscopes bandwidth is limited at 20MHz.

(9) A minimum of 47µF of ceramic capacitance is required across the input for proper operation. Locate the capacitor directly at V_{IN} of the device. An additional 220µF of bulk capacitance is recommended.

(10) The amount of required output capacitance varies depending on the output voltage. The amount of required capacitance must include at least 47µF of ceramic capacitance. Locate the capacitance close to the device. Adding additional capacitance close to the load improves the response of the regulator to load transients.

(11) When using both ceramic and non-ceramic output capacitance, the combined maximum must not exceed 1200µF.

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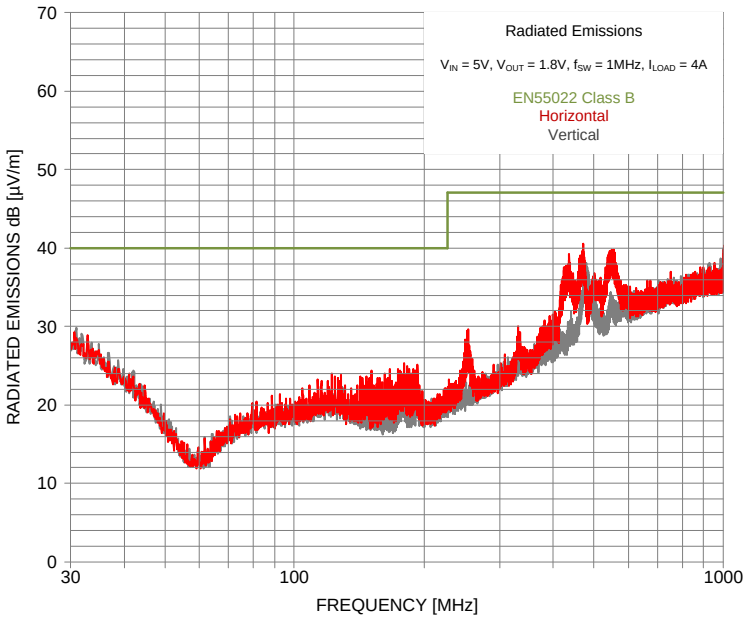
TYPICAL PERFORMANCE CURVES

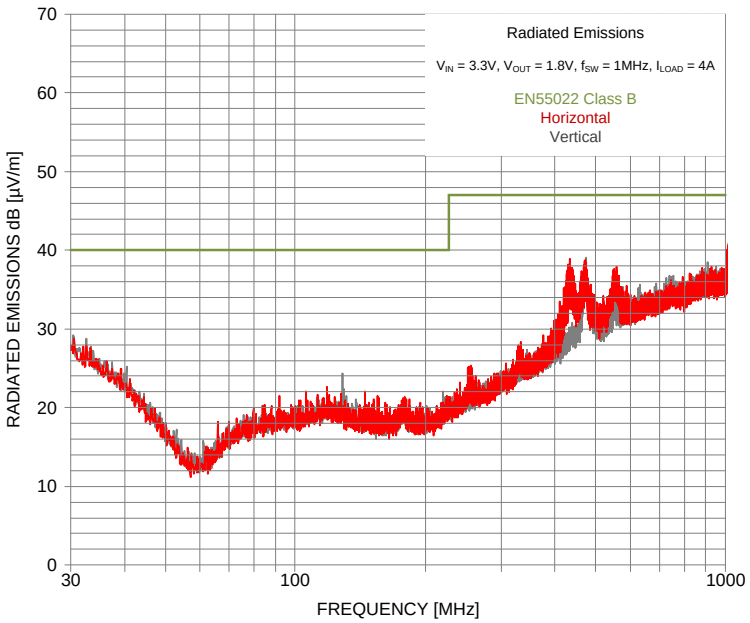
If not otherwise specified, the following conditions apply: V_{IN} = 3.3V - 5V; C_{IN} = 2 x 47µF X7R ceramic; C_{OUT} = 2x 47µF X7R ceramic, T_{AMB} = 25°C.

RADIATED EMISSIONS EN55022 (CISPR-22) CLASS B COMPLIANT

Measured on module with PCB and without external filters at 3m antenna distance



Measured on module with PCB and without external filters at 3m antenna distance



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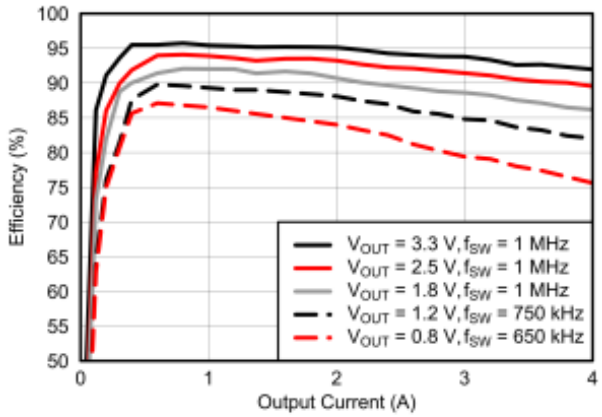
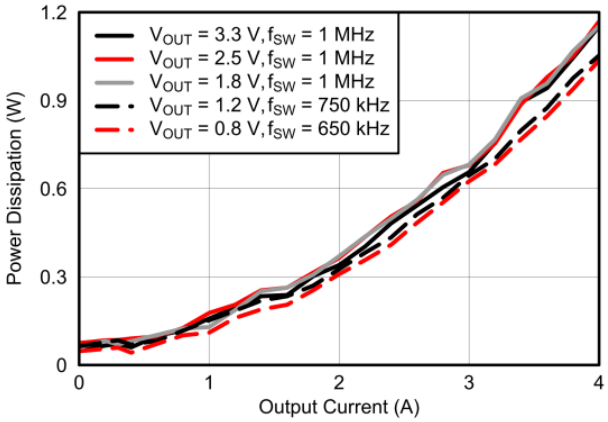
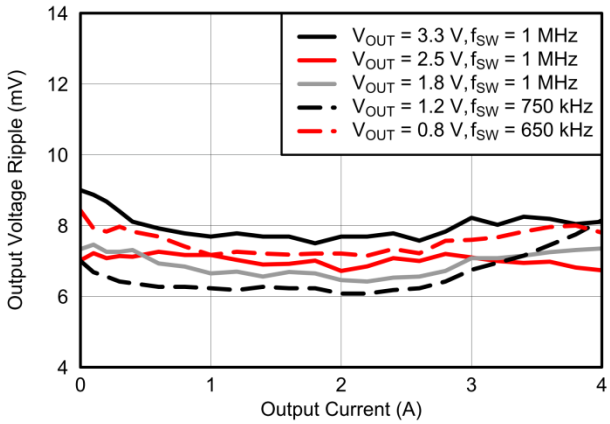
INPUT VOLTAGE 5V



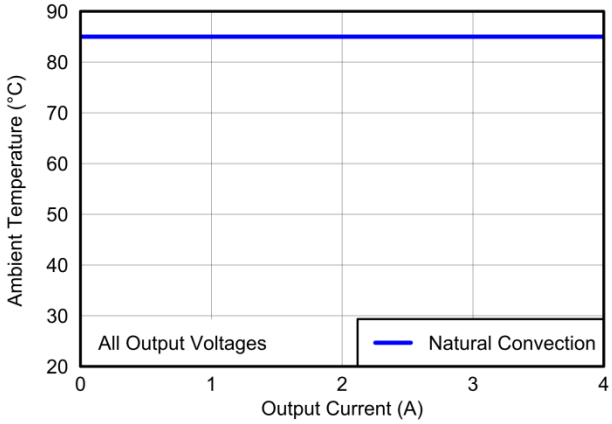
Efficiency vs. Output Current



Power Dissipation vs. Output Current



Voltage Ripple vs. Output Current



Safe Operating Area

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MagI³C Power Module

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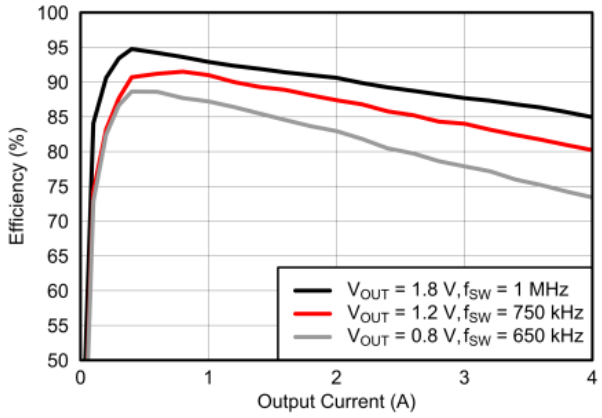
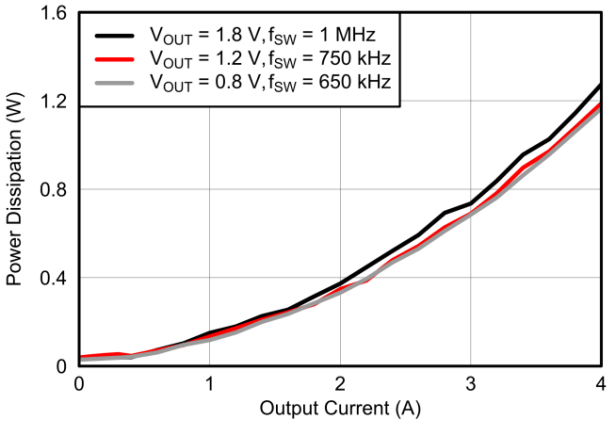
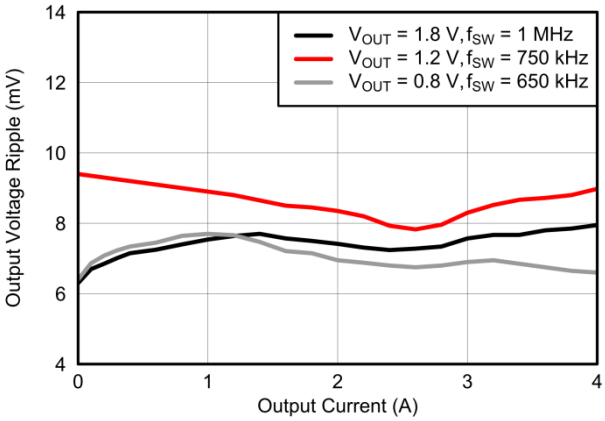
INPUT VOLTAGE 3.3V



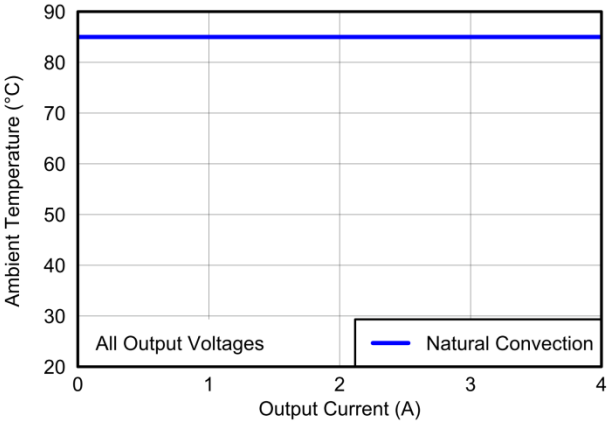
Efficiency vs. Output Current



Power Dissipation vs. Output Current



Voltage Ripple vs. Output Current



Safe Operating Area

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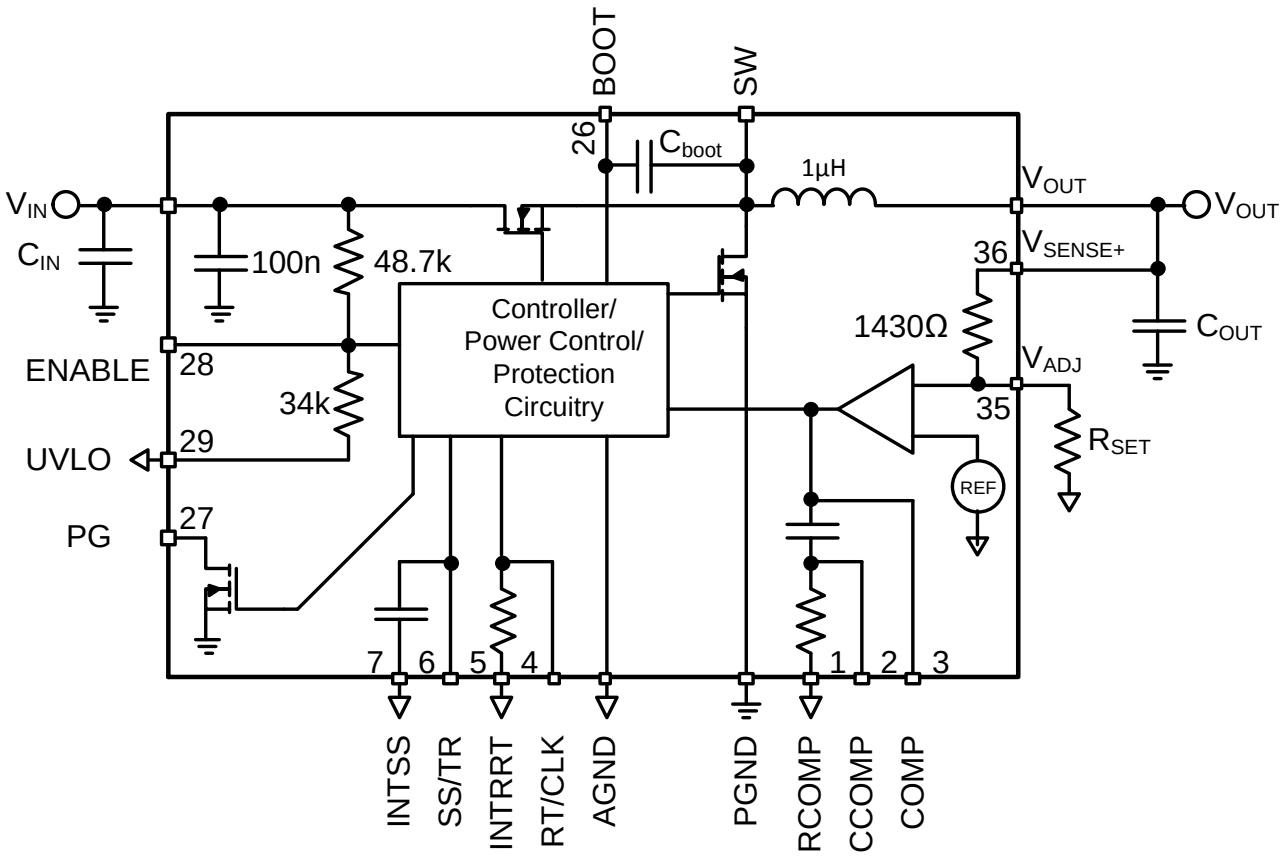
BLOCK DIAGRAM



CIRCUIT DESCRIPTION

The MagI³C Power Module 171020302 is based on a synchronous step down regulator with integrated MOSFETs and a power inductor. The control scheme is based on a Current Mode (CM) regulation loop.

The V_{OUT} of the regulator is divided with the feedback resistor network of internal 1430Ω and external R_{SET} and fed into the V_{ADJ} pin. The error amplifier compares this signal with the internal 0.803V reference. The error signal is amplified and controls the on-time of a fixed frequency pulse with generator. This signal drives the power mosfets.

The Current Mode architecture features a constant frequency during load steps. Only the on-time is modulated. It is internally compensated and stable with low ESR output capacitors and requires no external compensation network.

This architecture supports fast transient response and very small output ripple values of 10ths of millivolts are achieved.

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DESIGN FLOW

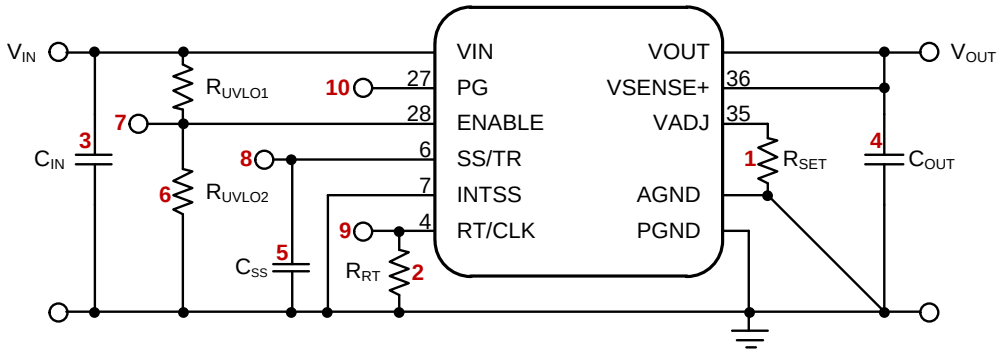
The next 10 simple steps will show how to select the external components to design your power application.

Essential Steps

1. Set output voltage
2. Set operating frequency
3. Select input capacitor
4. Select output capacitor

Optional Steps

5. Select soft start capacitor
6. Select under-voltage lockout divider
7. Enable / Disable
8. Voltage tracking
9. Synchronization to an external clock
10. Power Good



Step 1 Setting the output voltage (V_{OUT})

The output voltage is selected with a resistor divider across VADJ pin and AGND. The upper resistor of 1430 Ω of the feedback voltage resistor divider is internal to the module. The output voltage adjustment range is from 0.8V to 3.6V.

$$R_{SET} = \frac{0.8V * 1430\Omega}{V_{OUT} - 0.8V} (\Omega) \quad (1)$$

V_{OUT}	3.3V	3.0V	2.5V	1.8V	1.5V	1.2V	1.0V	0.8V
R_{SET} (E96)	453Ω	523Ω	665Ω	1130Ω	1620Ω	2870Ω	5620Ω	open

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Step 2 Setting the operating frequency (f_{SW})

The switching frequency must be selected according to input voltage, output voltage and load current for the best performance in loop regulation and transient response.

Note: R_{RT} open (f_{SW} = 500 kHz) is only allowed under specific conditions per below table!

		V_{IN} = 5V				V_{IN} = 3.3V	
OPERATING FREQUENCY [kHz]		I_{OUT} = 0 to 3.5A		I_{OUT} > 3.5A		I_{OUT} = 0 to 4A	
		V_{OUT} RANGE [V]		V_{OUT} RANGE [V]		V_{OUT} RANGE [V]	
	R_{RT} [kΩ]	MIN	MAX	MIN	MAX	MIN	MAX
500	open	0.8	1.4	0.8	1.0	0.8	2.2
550	3400	0.8	1.6	0.8	1.1	0.8	2.4
600	1800	0.8	1.8	0.8	1.2	0.8	2.5
650	1200	0.8	2.1	0.8	1.4	0.8	2.5
700	887	0.8	2.6	0.8	1.6	0.8	2.5
750	715	0.9	3.6	0.9	1.8	0.8	2.5
800	590	0.9	3.6	0.9	2.1	0.8	2.5
900	511	1.0	3.6	1.0	3.6	0.8	2.5
1000	348	1.2	3.6	1.2	3.6	0.8	2.5
1250	232	1.4	3.6	1.4	3.6	1.0	2.4
1500	174	1.7	3.6	1.7	3.6	1.1	2.3
1750	137	2.0	3.6	2.0	3.6	1.3	2.2
2000	113	2.3	3.4	2.3	3.3	1.5	2.2

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MagI³C Power Module

VDRM – Variable Step Down Regulator Module

Step 3 Select input capacitor (C_{IN})

The 171020302 MagI³C power module contains an 100nF internal input capacitor for good EMI performance. Additional input capacitance is required external to the MagI³C power module to handle the input ripple current of the application. Therefore an external input capacitance placed directly at the V_{IN} pin is required to handle the input ripple current of the application. The input capacitor can be several capacitors in parallel. Input capacitor selection is generally directed to satisfy the input ripple current requirements rather than by capacitance value. Input ripple current rating is dictated by the equation:

$$I_{C_{INRMS}} \approx \frac{1}{2} * I_{OUT} * \sqrt{\frac{D}{1-D}} \quad (2) \quad \text{where } D \approx \frac{V_{OUT}}{V_{IN}}$$

As a point of reference, the worst case ripple current will occur when the module is presented with full load current and when V_{IN} = 2 x V_{OUT}.

Recommended minimum input capacitance is 4.4µF X7R ceramic with a voltage rating at least 25% higher than the maximum applied input voltage for the application. It is also recommended that attention be paid to the voltage and temperature deratings of the capacitor selected. It should be noted that ripple current rating of ceramic capacitors may be missing from the capacitor data sheet and you may have to contact the capacitor manufacturer for this rating.

If the system design requires a certain minimum value of peak-to-peak input ripple voltage (ΔV_{IN}) be maintained then the following equation may be used:

$$C_{IN} \geq \frac{I_{OUT} * D * (1-D)}{f_{SW_{CCM}} * \Delta V_{IN}} \quad (3) \qquad \text{where } D \approx \frac{V_{OUT}}{V_{IN}} \qquad \text{CCM = continuous conduction mode}$$

Additional bulk capacitance with higher ESR may be required to damp any resonant effects of the input capacitance and parasitic inductance of the incoming supply lines.

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MagI³C Power Module
VDRM – Variable Step Down Regulator Module

Step 4 Select output capacitor (C_{OUT})

None of the required output capacitance is integrated within the module. At a minimum, the output capacitor must meet the worst case RMS current rating of $0.5 * I_{LRPP}$, as calculated in equation (4).

$$I_{LR_{PP}} = \frac{V_{OUT}*(V_{IN}-V_{OUT})}{1\mu H*f_{SW}*V_{IN}} \quad (4)$$

Beyond that, additional capacitance will reduce output ripple so long as the ESR is low enough to permit it. A minimum value of 10µF is generally required. Please consider the derating of the nominal capacitance value dependent on the DC voltage applied across it. Experimentation will be required if attempting to operate with a minimum value. Low ESR capacitors, such as ceramic and polymer electrolytic capacitors are recommended.

$$C_{OUT} \geq \frac{\Delta I_{OUT}*V_{ADJ}*L*V_{IN}}{4*V_{OUT}*(V_{IN}-V_{OUT})*\Delta V_{OUT}} \quad (5)$$

where ΔI_{OUT} is the load step in A, and ΔV_{OUT} is the maximum allowed voltage drop at the output voltage.

The ESR of the output capacitor affects the output voltage ripple. High ESR will result in larger V_{OUT} peak-to-peak ripple voltage. Furthermore, high output voltage ripple caused by excessive ESR can trigger the over-voltage protection monitored at the V_{SENSE+} pin. The ESR should be chosen to satisfy the maximum desired V_{OUT} peak-to-peak ripple voltage and to avoid over-voltage protection during normal operation. The following equations can be used:

$$ESR_{MAX} \leq \frac{V_{OUT_{RIPPLE}}}{I_{L_{RIPPLE}}} \quad (6)$$

Where $V_{OUT_{RIPPLE}}$ is the maximal wanted output ripple generated by ESR and $I_{L_{RIPPLE}}$ is the inductor ripple current calculated in equation (4).

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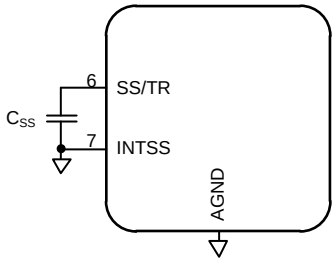
Step 5 Select soft-start capacitor (C_{SS})

Connecting the INTSS pin to AGND and leaving SS/TR pin open enables the internal soft start capacitor with a soft-start interval of approximately 1.1 ms. Adding additional capacitance between the SS/TR pin and AGND increases the soft-start time according to the table below.



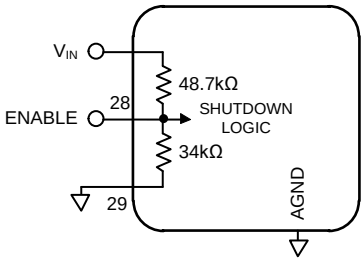
C_{SS} [nF]	Open	2.2	4.7	10	15	22	25
Soft Start [ms]	1.1	1.9	2.8	4.6	6.4	8.8	9.8

Step 6 Select under-voltage lockout divider

Pin 29 connected to analog ground

This connects the internal under-voltage lockout resistor divider. The enable rising threshold is typ. 1.25V. The enable falling threshold is at 1V max. Use at least 10% safety tolerance. For 3.3V input voltage use a rising threshold of below 3V which is achievable with pin 29 left open. An external under-voltage lockout resistor will set the rising threshold below 3V.

$V_{IN(UVLO)}$ rising threshold typ. [V]	3.14V
Hysteresis [mV]	300



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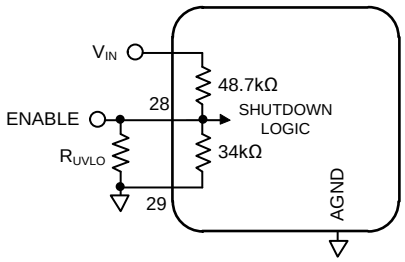
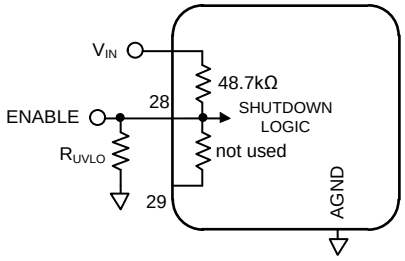
Pin 29 connected to AGND with additional resistor to adjust under-voltage lockout.



$V_{IN(UVLO)}$ rising threshold typ. [V]	3.25	3,5	3,75	4,0	4,25	4,5	4,75
R_{UVLO} [kΩ]	294	133	86.6	63.4	49.9	42.2	35.7
Hysteresis [mV]	325	335	345	355	365	375	385

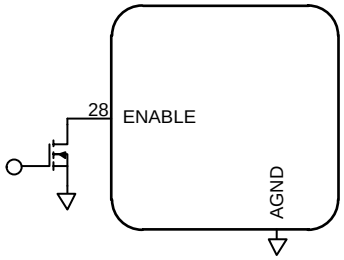
Pin 29 open with additional resistor to adjust under-voltage lockout for lower values.



$V_{IN(UVLO)}$ rising threshold typ. [V]	3.0	2.75	2.5	2.25
R_{UVLO} [kΩ]	34.0	39.7	47.5	60.4
Hysteresis [mV]	170	156	142	126

Step 7 Enable

Apply a voltage ≤ 1V to the enable pin to disable the device. Left open or set to ≥ 1.5V will enable the device. When disabeling use short leads to connect to AGND of the module. If not applicable use a transistor as below. The EN pin provides electrical on/off control of the device. Once the EN pin voltage exceeds the threshold voltage, the device starts operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low quiescent current state.



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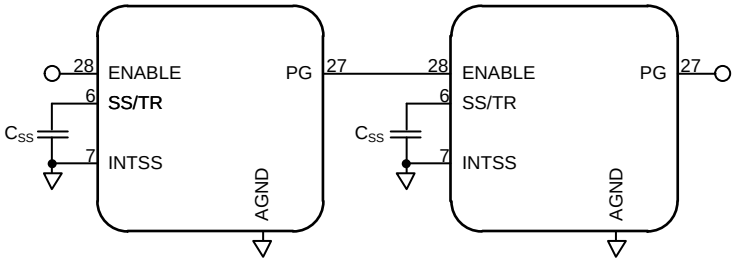
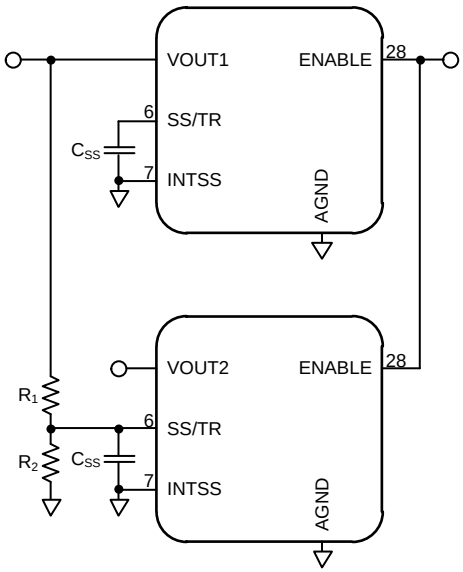
Step 8 Voltage tracking

Many of the common power supply sequencing methods can be implemented using the SS/TR, ENABLE and PG pins. The sequential voltage tracking is illustrated below using two devices. The PG pin of the first device is coupled to the ENABLE pin of the second device which enables the second power supply once the primary supply reaches regulation.



Simultaneous tracking

Simultaneous power supply sequencing can be implemented by connecting the resistor network of R_1 and R_2 as shown below to the output of the power supply that needs to be tracked or to another voltage reference source.



$$R_1 = \frac{V_{OUT2} * 12.6}{0.803}\ (\text{k}\Omega) \quad (7) \qquad R_2 = \frac{0.803 * R_1}{V_{OUT2} - 0.803}\ (\text{k}\Omega) \quad (8)$$

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Step 9 Synchronizing to an external clock

An internal phase locked loop (PLL) has been implemented to allow synchronization between 500 kHz and 2 MHz, and to easily switch from RT mode to CLK mode. To implement the synchronization feature, connect a square wave clock signal to the RT/CLK pin with a minimum pulse width of 75 ns. The maximum clock pulse width must be calculated using Equation 9. The clock signal amplitude must transition lower than 0.4 V and higher than 2.2 V. The start of the switching cycle is synchronized to the falling edge of RT/CLK pin. Applications requiring both RT mode and CLK mode, configure the device as shown in Figure 1. Before the external clock is present, the device works in RT mode and the switching frequency is set by the RT resistor (R_{RT}). When the external clock is present, the CLK mode overrides the RT mode. The device switches from RT mode to CLK mode and the RT/CLK pin becomes high impedance as the PLL starts to lock onto the frequency of the external clock. The device will lock to the external clock frequency approximately 15 µs after a valid clock signal is present. It is not recommended to switch from CLK mode back to RT mode because the internal switching frequency drops to a lower frequency before returning to the switching frequency set by the RT resistor.

$$\text{Maximum clock pulse width} = \frac{0.75*(1-\frac{V_{OUT}}{V_{INMIN}})}{f_{SW}} \quad (9)$$

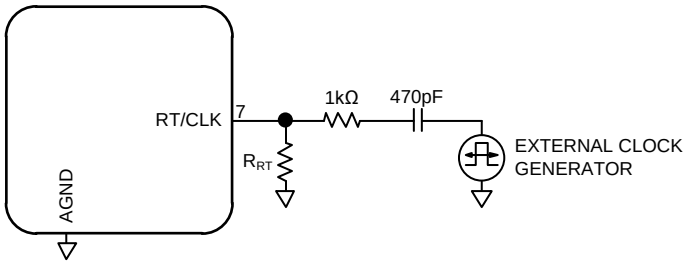
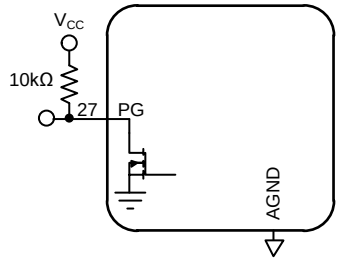


Figure 1

Step 10 Power Good

The PG pin is an open drain output. Once the voltage on the SENSE+ pin is between 93% and 107% of the nominal value, the PG pin pull-down is released and the pin floats. The recommended pull-up resistor value is between 10 kΩ and 100 kΩ to a voltage source that is 6 V or less. The PG pin is in a defined state once V_{IN} is greater than 1.2 V, but with reduced current sinking capability. The PG pin achieves full current sinking capability once the V_{IN} pin is above 2.95V. The PG pin is pulled low when the voltage on SENSE+ is lower than 91% or greater than 109% of the nominal set voltage. Also, the Power Good pin is pulled low if the input UVLO or thermal shutdown is asserted, or if the ENABLE pin is pulled low.



V_{CC} = V_{IN} or other supply voltage below 6V

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MagI³C Power Module
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PROTECTIVE FEATURES

Over temperature protection (OTP)

For protection against load faults, the MagI³C Power Module incorporates cycle-by-cycle current limiting. During an overcurrent condition the output current is limited and the output voltage is reduced. As the output voltage drops more than 9% below the set point, the PG signal is pulled low. If the output voltage drops more than 25%, the switching frequency is reduced to reduce power dissipation within the device. When the overcurrent condition is removed, the output voltage returns to the established voltage.

Over current protection (OCP)

The junction temperature of the MagI³C power module should not be allowed to exceed its maximum ratings. Thermal protection is implemented by an internal Thermal Shutdown circuit which activates at 175°C (typ) causing the device to enter a low power standby state. In this state the main MOSFET remains off causing V_{OUT} to fall, and additionally the C_{SS} capacitor is discharged to ground. Thermal protection helps prevent catastrophic failures for accidental device overheating. When the junction temperature falls back below 160° the SS pin is released, V_{OUT} rises smoothly, and normal operation resumes.
Applications requiring maximum output current especially those at high input voltage may require additional derating at elevated temperatures.

Short circuit protection (SCP)

The short circuit protection is realized via the cycle by cycle current limiting. The short circuit protection is indefinite with a recovery at the following switching cycle if the short circuit is removed.

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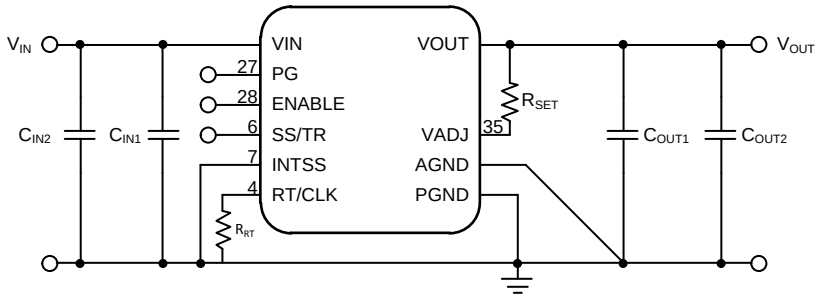
TYPICAL SCHEMATIC



INPUT	OUTPUT	C_{IN2}	C_{IN1}	R_{RT}	R_{SET}	C_{OUT1}	C_{OUT2}
5V	3.3V	220µ	47µF X5R	174kΩ	459Ω	47µ X5R	-
5V	2.5V	220µ	47µF X5R	174kΩ	673Ω	47µ X5R	47µ X5R
5V	1.8V	220µ	47µF X5R	348kΩ	1150Ω	47µ X5R	100µF
5V	1.5V	220µ	47µF X5R	348kΩ	1650Ω	47µ X5R	100µF
5V	1.2V	220µ	47µF X5R	715kΩ	2870Ω	47µ X5R	100µF
5V	1.0V	220µ	47µF X5R	715kΩ	5830Ω	47µ X5R	100µF
5V	0.8V	220µ	47µF X5R	1200kΩ	Open	47µ X5R	100µF
3.3V	1.8V	220µ	47µF X5R	348kΩ	1150Ω	47µ X5R	100µF
3.3V	1.5V	220µ	47µF X5R	348kΩ	1650Ω	47µ X5R	100µF
3.3V	1.2V	220µ	47µF X5R	715kΩ	2870Ω	47µ X5R	100µF
3.3V	1.0V	220µ	47µF X5R	715kΩ	5830Ω	47µ X5R	100µF
3.3V	0.8V	220µ	47µF X5R	1200kΩ	Open	47µ X5R	100µF

C_{IN2} and C_{OUT2} ≥ 100µF are polymer tantalum types.

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MagI³C Power Module

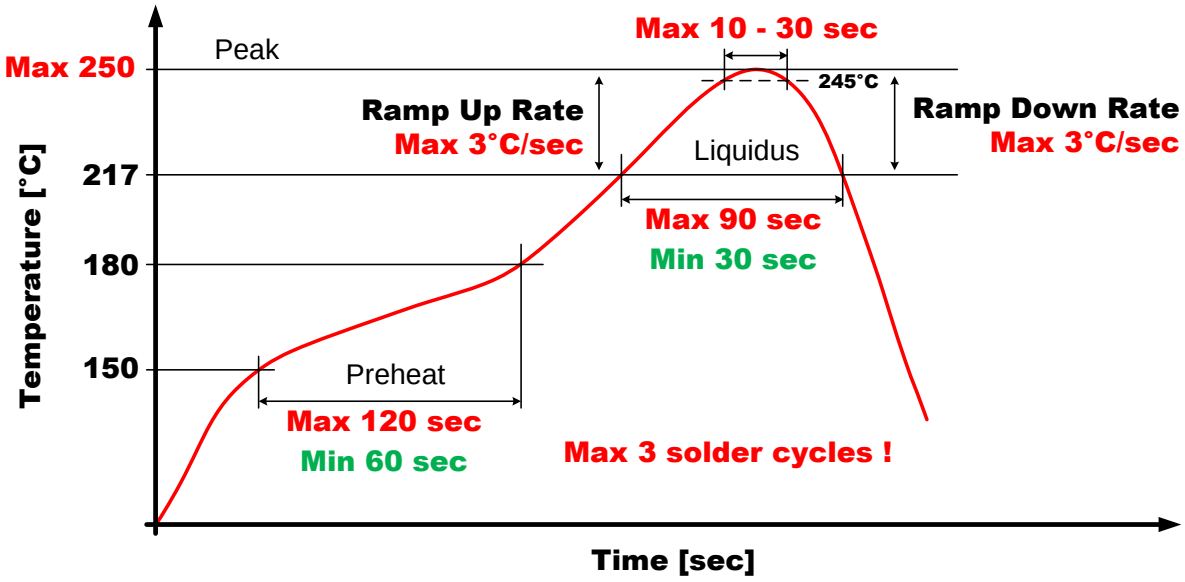
VDRM – Variable Step Down Regulator Module

HANDLING RECOMMENDATIONS

1. The power module is classified as MSL3 (JEDEC Moisture Sensitivity Level 3) and requires special handling due to moisture sensitivity (JEDEC J-STD033).
2. The parts are delivered in a sealed bag (Moisture Barrier Bags = MBB) and should be processed within one year.
3. When opening the moisture barrier bag check the Humidity Indicator Card (HIC) for color status. Bake parts prior to soldering in case indicator color has changed according to the notes on the card.
4. Parts must be processed after 168 hour (7 days) of floor life. Once this time has been exceeded, bake parts prior to soldering per JEDEC J-STD033 recommendation.

SOLDER PROFILE

1. Only Pb-Free assembly is recommended according to JEDEC J-STD020.
2. Measure the peak reflow temperature of the MagI³C power module in the middle of the top view.
3. Ensure that the peak reflow temperature does not exceed 245°C ±5°C as per JEDEC J-STD020.
4. The reflow time period during peak temperature of 245°C ±5°C must not exceed 30 seconds.
5. Reflow time above liquidus (217°C) must not exceed 90 seconds.
6. Maximum ramp up is rate 3°C per second.
7. Maximum ramp down rate is 3°C per second.
8. Reflow time from room (25°C) to peak must not exceed 8 minutes as per JEDEC J-STD020.
9. **Maximum numbers of reflow cycles is three.**
10. **For minimum risk, solder the module in the last reflow cycle of the PCB production.**
11. For soldering process please consider lead material copper (Cu) and lead finish tin (Sn).
12. For solder paste use a standard SAC Alloy such as SAC 305, type 3 or higher.
13. Below profile is valid for convection reflow only.
14. Other soldering methods (e.g.vapor phase) are not verified and have to be validated by the customer on his own risk.



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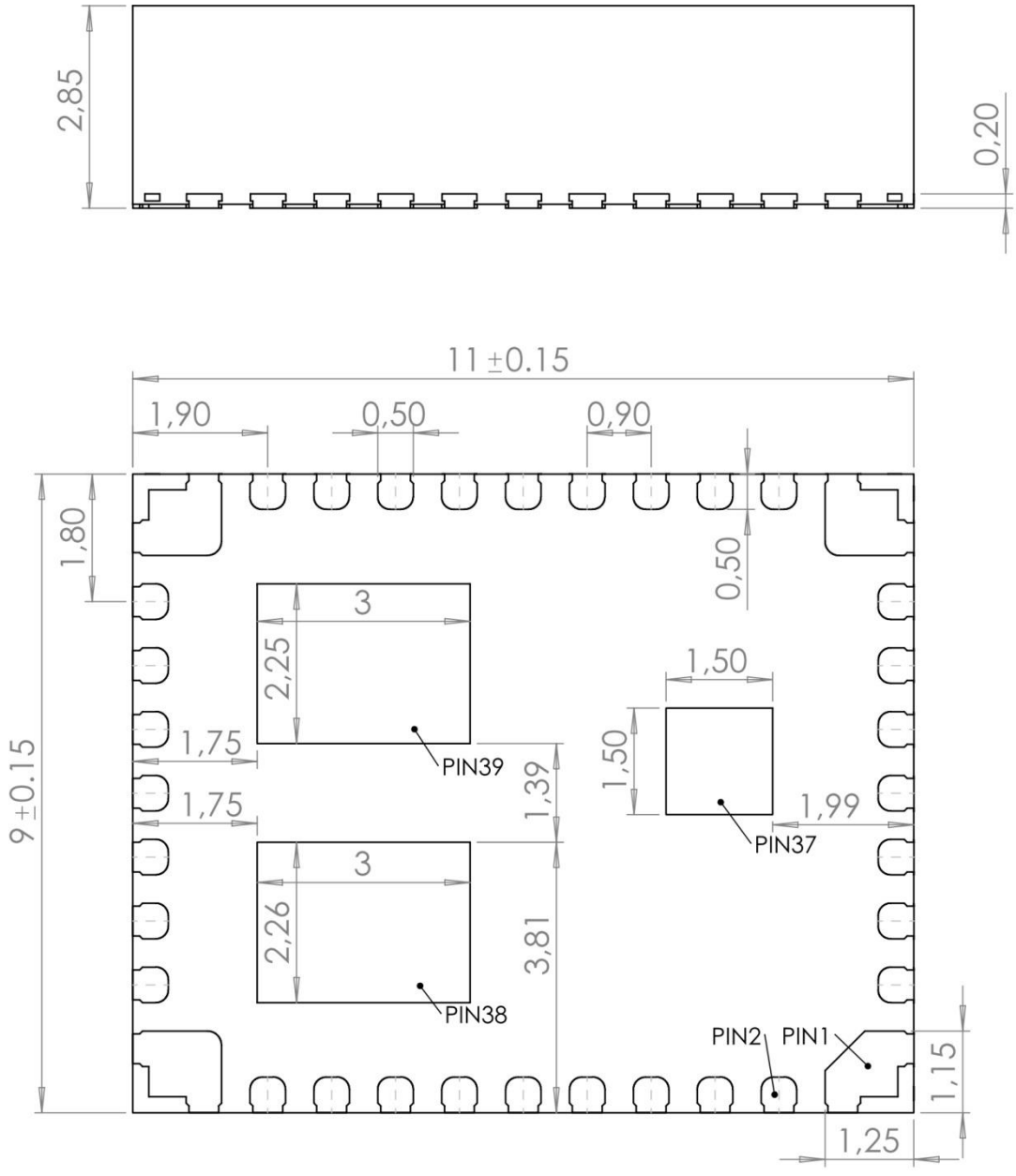
MagI³C Power Module

VDRM – Variable Step Down Regulator Module

PHYSICAL DIMENSIONS



Bottom View

all dimensions in mm

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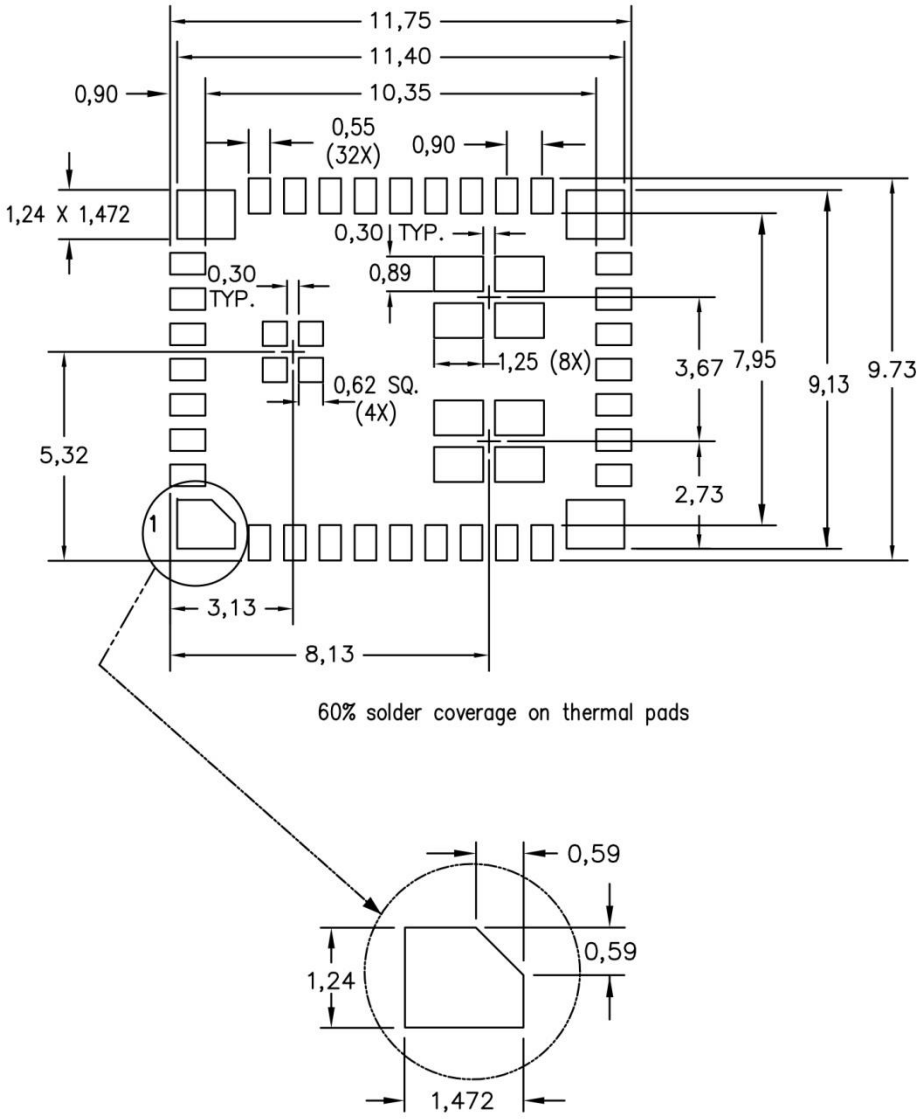
MagI³C Power Module

VDRM – Variable Step Down Regulator Module

EXAMPLE STENCIL DESIGN



Stencil thickness 0.125mm

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DOCUMENT HISTORY

Revision	Date	Description	Comment
0.1	31.03.2015	Preliminary version	

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CAUTIONS AND WARNINGS

The following conditions apply to all goods within the product series of MagI³C of Würth Elektronik eiSos GmbH & Co. KG:

General:
All recommendations according to the general technical specifications of the data-sheet have to be complied with.

The usage and operation of the product within ambient conditions which probably alloy or harm the component surface has to be avoided.

The responsibility for the applicability of customer specific products and use in a particular customer design is always within the authority of the customer. All technical specifications for standard products do also apply for customer specific products.

Residual washing varnish agent that is used during the production to clean the application might change the characteristics of the body, pins or termination. The washing varnish agent could have a negative effect on the long term function of the product.
Direct mechanical impact to the product shall be prevented as the material of the body, pins or termination could flake or in the worst case it could break. As these devices are sensitive to electrostatic discharge customer shall follow proper IC Handling Procedures.

Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Würth Elektronik eiSos GmbH & Co. KG components in its applications, notwithstanding any applications-related information or support that may be provided by Würth Elektronik eiSos GmbH & Co. KG. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Customer will fully indemnify Würth Elektronik eiSos and its representatives against any damages arising out of the use of any Würth Elektronik eiSos GmbH & Co. KG components in safety-critical applications.

Product specific:
Follow all instructions mentioned in the datasheet, especially:
- The solder profile has to comply with the technical reflow or wave soldering specification, otherwise this will void the warranty.
- All products are supposed to be used before the end of the period of 12 months based on the product date-code.
- Violation of the technical product specifications such as exceeding the absolute maximum ratings will void the warranty.
- It is also recommended to return the body to the original moisture proof bag and reseal the moisture proof bag again.
- ESD prevention methods need to be followed for manual handling and processing by machinery.

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MagI³C Power Module

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IMPORTANT NOTES

The following conditions apply to all goods within the product range of Würth Elektronik eiSos GmbH & Co. KG:

1. General Customer Responsibility
Some goods within the product range of Würth Elektronik eiSos GmbH & Co. KG contain statements regarding general suitability for certain application areas. These statements about suitability are based on our knowledge and experience of typical requirements concerning the areas, serve as general guidance and cannot be estimated as binding statements about the suitability for a customer application. The responsibility for the applicability and use in a particular customer design is always solely within the authority of the customer. Due to this fact it is up to the customer to evaluate, where appropriate to investigate and decide whether the device with the specific product characteristics described in the product specification is valid and suitable for the respective customer application or not. Accordingly, the customer is cautioned to verify that the datasheet is current before placing orders.

2. Customer Responsibility related to Specific, in particular Safety-Relevant Applications
It has to be clearly pointed out that the possibility of a malfunction of electronic components or failure before the end of the usual lifetime cannot be completely eliminated in the current state of the art, even if the products are operated within the range of the specifications. In certain customer applications requiring a very high level of safety and especially in customer applications in which the malfunction or failure of an electronic component could endanger human life or health it must be ensured by most advanced technological aid of suitable design of the customer application that no injury or damage is caused to third parties in the event of malfunction or failure of an electronic component.

3. Best Care and Attention
Any product-specific notes, warnings and cautions must be strictly observed.

4. Customer Support for Product Specifications
Some products within the product range may contain substances which are subject to restrictions in certain jurisdictions in order to serve specific technical requirements. Necessary information is available on request. In this case the field sales engineer or the internal sales person in charge should be contacted who will be happy to support in this matter.

5. Product R&D
Due to constant product improvement product specifications may change from time to time. As a standard reporting procedure of the Product Change Notification (PCN) according to the JEDEC-Standard we inform about minor and major changes. In case of further queries regarding the PCN, the field sales engineer or the internal sales person in charge should be contacted. The basic responsibility of the customer as per Section 1 and 2 remains unaffected.

6. Product Life Cycle
Due to technical progress and economical evaluation we also reserve the right to discontinue production and delivery of products. As a standard reporting procedure of the Product Termination Notification (PTN) according to the JEDEC-Standard we will inform at an early stage about inevitable product discontinuance. According to this we cannot guarantee that all products within our product range will always be available. Therefore it needs to be verified with the field sales engineer or the internal sales person in charge about the current product availability expectancy before or when the product for application design-in disposal is considered. The approach named above does not apply in the case of individual agreements deviating from the foregoing for customer-specific products.

7. Property Rights
All the rights for contractual products produced by Würth Elektronik eiSos GmbH & Co. KG on the basis of ideas, development contracts as well as models or templates that are subject to copyright, patent or commercial protection supplied to the customer will remain with Würth Elektronik eiSos GmbH & Co. KG. Würth Elektronik eiSos GmbH & Co. KG does not warrant or represent that any license, either expressed or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, application, or process in which Würth Elektronik eiSos GmbH & Co. KG components or services are used.

8. General Terms and Conditions
Unless otherwise agreed in individual contracts, all orders are subject to the current version of the “General Terms and Conditions of Würth Elektronik eiSos Group”, last version available at www.we-online.com.

